A NEW CONFIGURATION PROVIDING NEGATIVE RESISTANCE AT A HIGHER FREQUENCY THAN THAT OF THE NEGATIVE RESISTANCE DEVICE BY ITSELF

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ABSTRACT

It is shown that the combination of a negative resistance at frequency w and a varactor frequency multiplier/divider can produce a negative resistance at frequency 2w. Experimental results are presented on an injection locked oscillator at 2w using this combination.

INTRODUCTION

The input impedance to a lossless varactor frequency doubler resonated at the input and output frequency can be approximated by the equation[1]

$$R(w) = (K/wC)^2/RL(2w) \quad (1)$$

where, RL(2w) is the load impedance of the frequency doubler at 2w, the output frequency, R(w) is the input impedance at the input frequency w as seen by the input signal generator, C is the minimum capacitance of the varactor diode and K is a constant. Similarly the input impedance of a lossless divide by two circuit can be approximated by the equation:

$$R'(2w) = (K'/wC)^2/RL'(w) \quad (2)$$

where, RL'(w) is the load impedance of the frequency divide by two circuit at frequency w, R'(2w) is the input impedance of the divider at frequency 2w and K' is a constant. It is shown in Appendix 1 that the equations for the varactor multiplier and divider are such that eq.1 &2 above also hold when RL and RL' are negative. We see from eq.2 that if a frequency divide by two circuit is terminated in a negative resistance at frequency w, then we will see a negative resistance at the input terminals of the divider at 2w.[2] It therefore follows that a negative resistance amplifier or an injection locked oscillator can be built using the configuration[2] shown in fig.1. The configuration shown in fig.1 also applies to high order dividers such as divide by three etc. The configuration of fig.1 allows the use of a negative resistance device which operates at a lower frequency to provide a negative resistance at a harmonic frequency. Thus for example a 2 Ghz. transistor could be used in combination with a divide by three circuit to produce a negative resistance amplifier at 6 Ghz. It is well known that a properly designed varactor doubler also operates as a frequency divide by two circuit when the output frequency of the doubler is applied to the output port of the doubler and the input port is terminated. This is also true for high order multipliers. We will therefore, refer to the circuit as a multiplier/divider.

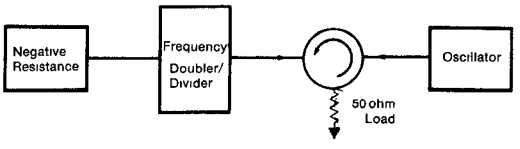

Figure 1. Basic Circuit Configuration

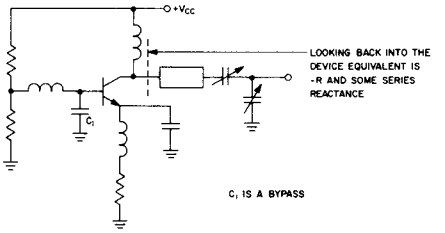

Figure 2. Transistor Negative Resistance Circuit

EXPERIMENTAL RESULTS

In order to verify the theory an injection locked oscillator was built according to fig.1. The circuit was built at UHF frequencies and consisted of a 305 Mhz. transistor oscillator terminated in a varactor frequency multiplier/divider. The 305 Mhz. oscillator circuit is shown in fig.2. Looking into port 1 fig.2 one "sees" a negative resistance at 305Mhz and hence when port 1 is terminated in 50 ohms the circuit oscillates at 305 Mhz. with an output power of 300 mw. The locking range of the oscillator was measured and is shown in fig. 3 where the ratio of the locking range to center frequency is plotted vs. the ratio of the locking power to the oscillator output power. A varactor frequency doubler/ divider was then connected to port 1 of the oscillator. Table 1a shows the efficiency of this circuit as a divider as well as the level of other harmonics present at the output port of the divider. Table 1b shows the efficiency of the circuit as a frequency doubler and the level of other harmonics at the output of the doubler. It should be noted that the circuit was tuned for best performance as a divider and then measured as a doubler without further tuning. The output power of the oscillator doubler/divider combination was 200 mw. at 610 Mhz. The locking range of the combination was measured using an injected signal at a frequency in the vicinity of 610 Mhz. The results are plotted in fig. 3. As can be seen from the figure the the normalized locking range is less for the combination then for the oscillator alone. There is however,a significant range over which the combination can be injection locked.

CONCLUSION

A new configuration has been presented which produces negative resistance at a higher frequency than the device by itself. The theory was verified by an experimental phase locked oscillator.

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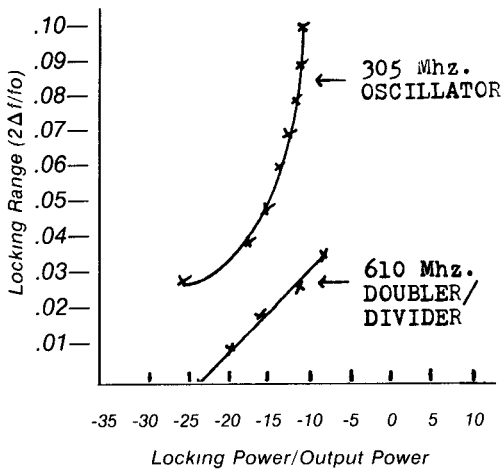

Figure 3 Locking Range vs Locking Power

Ref.1 - R.H. Johnston and A.R. Boothroyd, "Charge Storage Frequency Multipliers", Proc. IEEE vol. 56 page 169 eq.5.
Ref.2 - U.S. Patent No. 4,025,872

APPENDIX

The solutions for doublers and high order multipliers using punch-through varactors (also known as bi-mode varactors and step recovery diodes) has been given in the literature.(Ref.1). We will show in this appendix that if one connects a negative resistance at frequency w to the input terminals of a punch-through varactor times-N multiplier, a negative resistance appears at the output terminals of the multiplier at frequency Nw. We will further show that if the value of the negative resistance is equal to the input impedance of the multiplier when the multiplier is terminated in P_I, then the value of the negative resistance appearing at the output terminals of the multiplier will be equal to R_L. It therefore follows, that a multiplier designed for a load and source impedance of 50 ohms will exhibit a negative resistance of 50 ohms when a negative resistance of 50 ohms is connected to the input terminals. Under these conditions the charge waveform across the diode is the same as when the diode is operated as a conventional multiplier.

The voltage-charge relationship for a lossless punch-through varactor is given by:

$$V = \begin{cases} q & q \geq 0 \\ 0 & q \leq 0 \end{cases} \qquad \text{A.1}$$

where V and q are normalized voltage and charge with maximum values of 1.It has been found that the charge waveform for doublers and high order multipliers which yields the highest efficiency is positive for the condition $0 \leq \theta \leq 180^\circ$ and negative for the condition $180^\circ \leq \theta \leq 360^\circ$, where θ=wt. We can therefore write eq. A.1 for these optimum charge waveforms as:

$$V = \begin{cases} q & 0 \leq \theta \leq 180^\circ \\ 0 & 180^\circ \leq \theta \leq 360^\circ \end{cases} \qquad \text{A.2}$$

The charge waveform for a times-N multiplier can be written in the form

$$q(t) = \sum_{k=1}^{N} 2Q_k \sin(kwt) = \sum_{k=1}^{N} 2Q_k \sin k\theta \qquad \text{A.3}$$

The voltage across the diode and the current into the diode can be written as:

$$V(\theta) = \Sigma V_{kc} \cos k\theta + V_{ks} \sin k\theta \qquad \text{A.4a}$$

$$i(\theta) = \sum I_k \cos k\theta = \sum_{k=1}^{N} 2kwQ_k \cos k\theta \qquad \text{A.4b}$$

The Fourier coefficients of the voltage waveform can be found by substituting eq.A.4 into eq. A.2 and expanding in a Fourier series. The values of V_{1c} and V_{2c} for the frequency doubler are found to be:

$$V_{1c} = 8Q_2/3\pi \qquad V_{2c} = -4Q_1/3\pi \qquad \text{A.5}$$

It can be seen from eqs. A.4a and A.4b that V_{kc} and I_k are in phase while V_{ks} and I_{ks} are in quadrature. Thus V_{ks} gives rise to a reactive component which we will assume is resonated in the multiplier while V_{kc} gives rise to a real impedance and contributes to the power at kw. The power into and out of the lossless varactor is:

$$P = wQ_1V_{1c} = 2wQ_2V_{2c} = 8wQ_1Q_2/3\pi \qquad \text{A.6}$$

If the doubler is terminated in a load impedance with real part R_L at frequency 2w (and imaginary part necessary to resonate the varactor at 2w) then:

$$R_L = V_{2c}/-I_2 = Q_1/(3\pi wQ_2) \qquad \text{A.7}$$

The input impedance to the doubler at frequency w is:

$$R_{in} = V_{1c}/I_1 = 4Q_2/(3\pi wQ_1) \qquad \text{A.8}$$

If on the other hand the doubler has its input terminated with a negative resistance -R at frequency w then

$$-R = V_{1c}/-I_1 \qquad \text{A.9a}$$

and

$$R = V_{1c}/I_1 = 4Q_2/(3\pi wQ_1) \qquad \text{A.9b}$$

The impedance seen looking into the output terminal of the doubler at 2w is given by:

$$R'_{in} = V_{2c}/I_2 = -Q_1/(3\pi wQ_2) \qquad \text{A.10}$$

Combining eqs. A.9 and A.10 yields:

$$R'_{in}(2w) = -R(Q_1/2Q_2)^2 \qquad \text{A.11}$$

We thus see that terminating the diode in a negative resistance at w yields a negative resistance at 2w. Comparing eqs. A.7, A.8, A.9 and A.10 we see that if the value of the negative resistance (eq. A.9) is equal to the value of the input impedance of the

doubler (eq. A.8) then the ratio of Q_2/Q_1 is the same for both cases. The value of the negative resistance at frequency 2w (eq. A.10) is then equal to the load impedance R_L of the doubler (eq. A.7).

The values of V_{1c}, V_{2c} and V_{3c} for the frequency tripler assuming a lossless idler ($V_{2c}=0$) are found from eqs. A.4 and A.2.

$$V_{1c} = 8Q_2/3\pi$$
$$V_{2c} = 12Q_3/5\pi - 4Q_1/3\pi = 0 \qquad \text{A.12}$$
$$V_{3c} = -8Q_2/5\pi$$

If the tripler is terminated in a load impedance R_L at 3w (and imaginery part necessary to resonate the varactor) then

$$R_I = V_{3c}/-I_3 = 4Q_2/15\pi Q_3 = 12Q_2/25\pi wQ_1$$
$$R_{in} = V_{1c}/I_1 = 4Q_2/3\pi wQ_1 \qquad \text{A.13}$$

Combining eqs. A.13 we find that

$$R_{in} = 25R_L/9 = R_L(3Q_3/Q_1)^2 \qquad \text{A.14}$$

If on the other hand the tripler has its input terminated in a negative resistance -R then:

$$-R = V_{1c}/I_1 \qquad \text{A.15a}$$

and

$$R = V_{1c}/I_1 = 4Q_2/(3\pi wQ_1) \qquad \text{A.15b}$$

The impedance seen looking into the output terminals of the tripler at 3w is given by

$$R'_{in}(3w) = -25R/9 \qquad \text{A.16}$$

We thus see that terminating the input terminals of a tripler in a negative resistance at w yields a negative resistance at 3w.

Similar analysis shows that the same conclusions hold for higher order multipliers.

Ref. 1. D.H. Steinbrecher, "Efficiency Limits for Tuned Harmonic Multipliers with punch-through Varactors," Int. Solid-State Circuits Conference, Dig. Tech. Papers, Feb. 1967.